Fig. 1

(PRIOR ART)

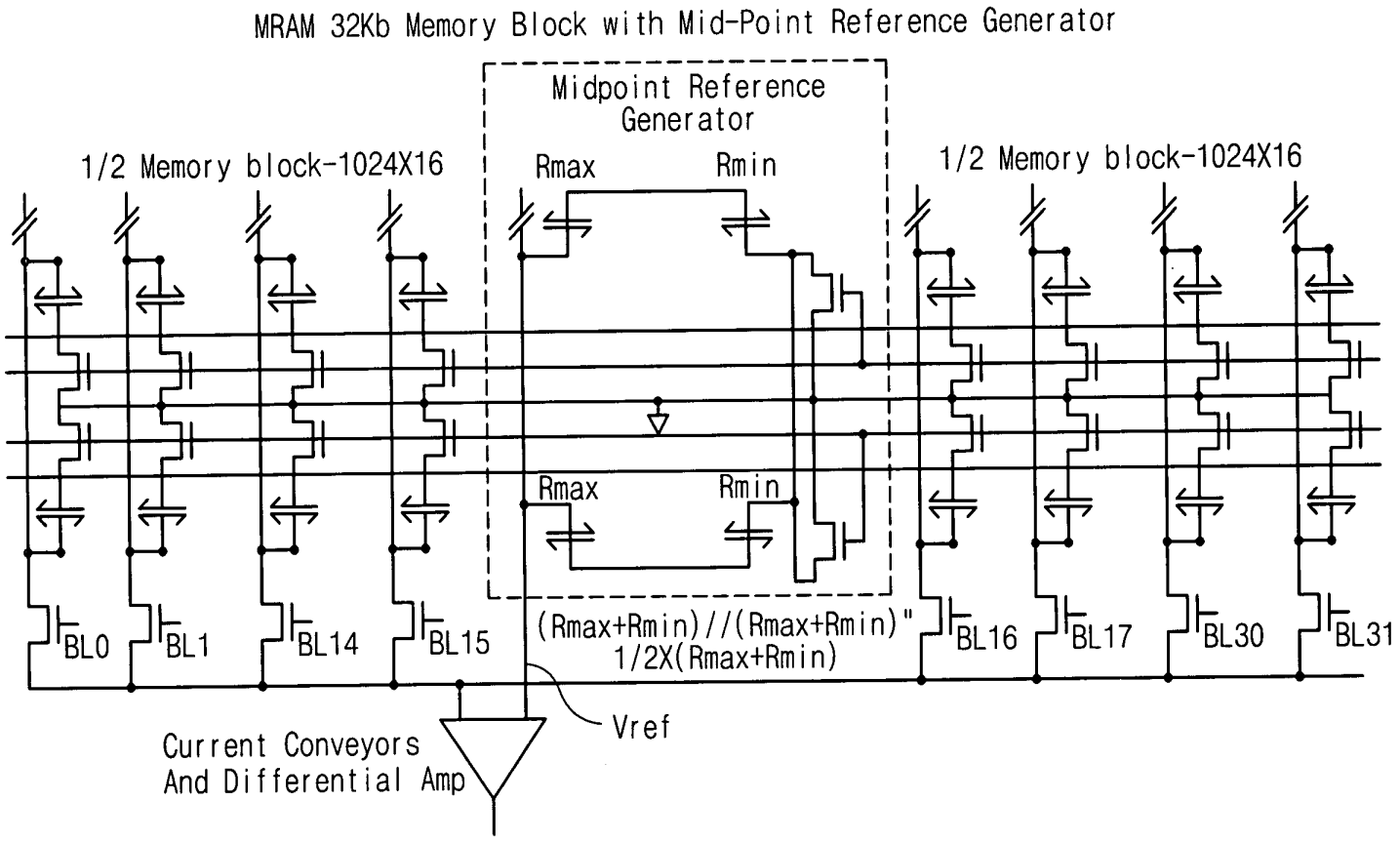


Fig. 2

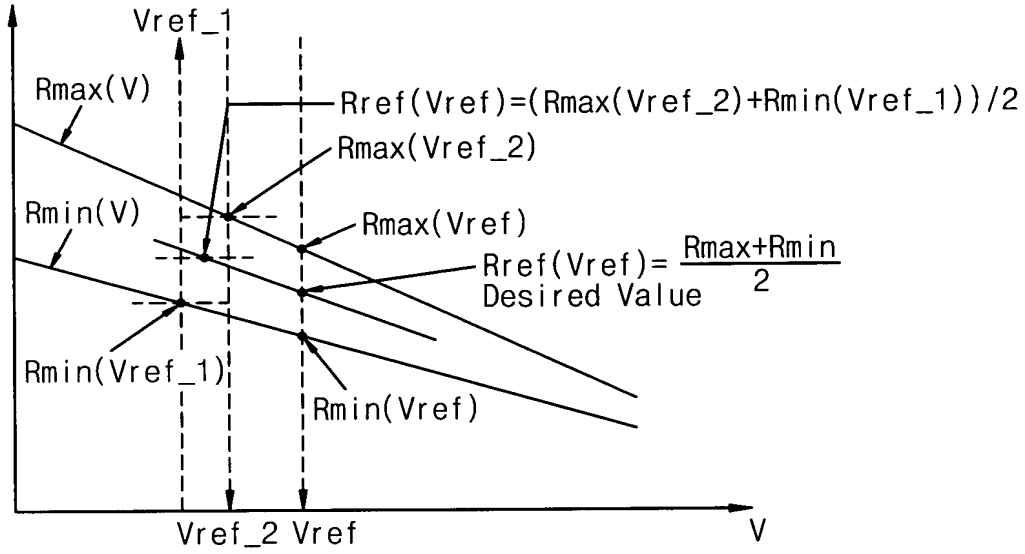

Vref_1
Rmax(V)
Rref(Vref)=(Rmax(Vref_2)+Rmin(Vref_1))/2
Rmax(Vref_2)
Rmin(V)
Rmax(Vref)
Rref(Vref)= Rmax+Rmin / 2
Desired Value
Rmin(Vref_1)
Rmin(Vref)
Vref_2 Vref
V

Fig. 3

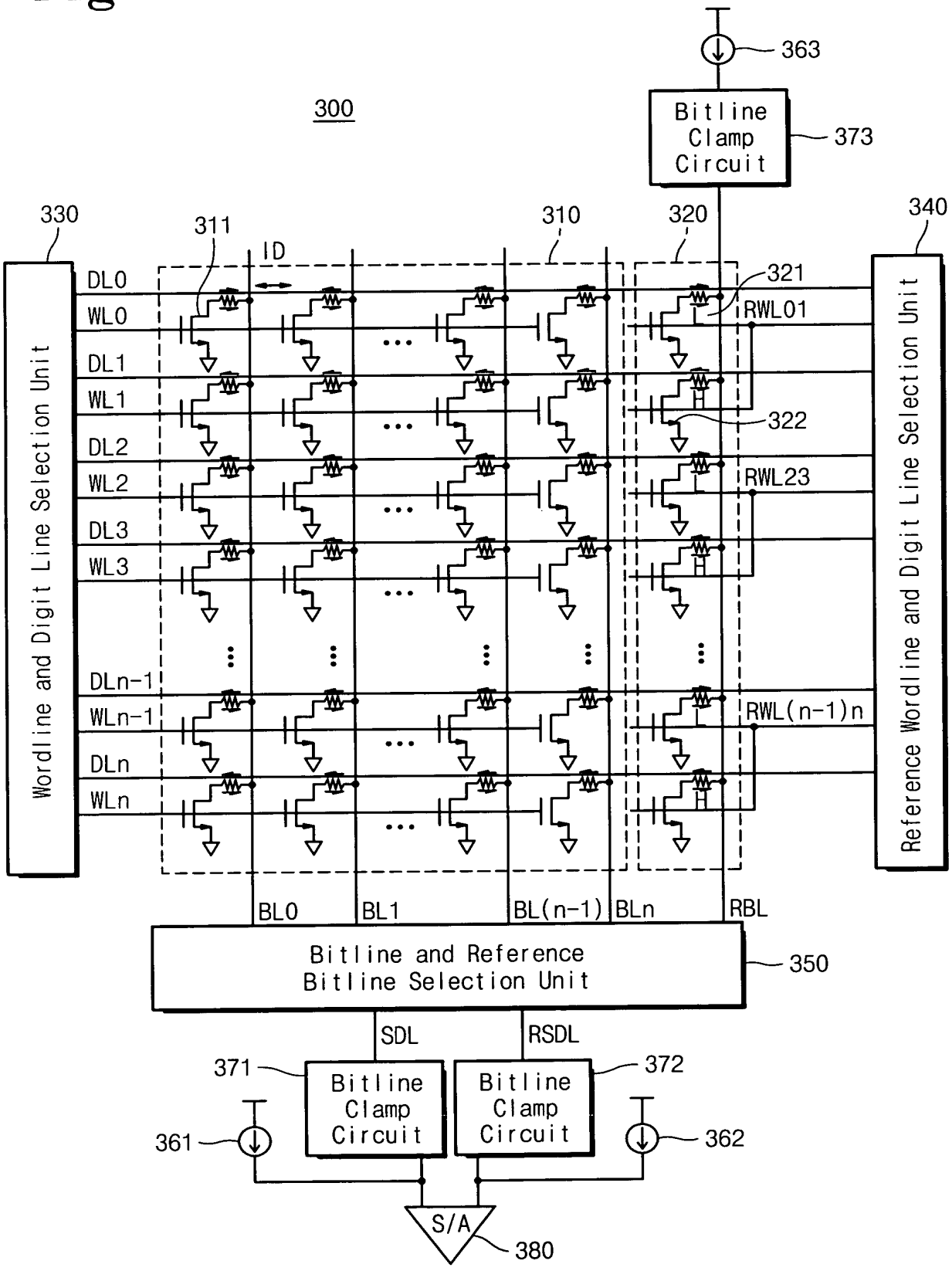

300
363
Bitline Clamp Circuit
373
330
311
ID
310
320
340
321
RWL01
322
RWL23
RWL(n-1)n
Wordline and Digit Line Selection Unit
Reference Wordline and Digit Line Selection Unit
DL0
WL0
DL1
WL1
DL2
WL2
DL3
WL3
DLn-1
WLn-1
DLn
WLn
BL0
BL1
BL(n-1)
BLn
RBL
Bitline and Reference Bitline Selection Unit
350
SDL
RSDL
371
372
Bitline Clamp Circuit
Bitline Clamp Circuit
361
362
S/A
380

Fig. 4

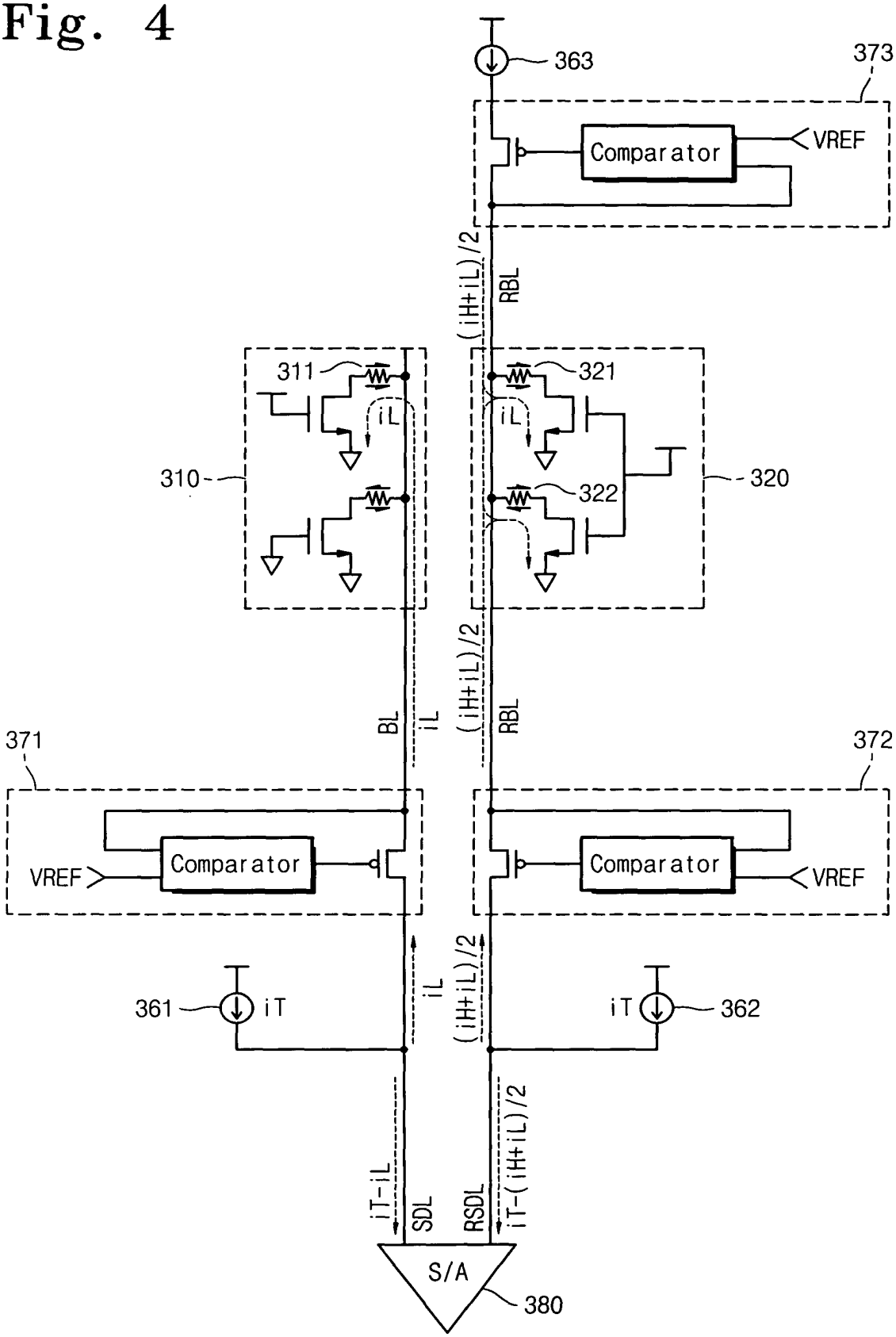

363
373
Comparator
VREF
(iH+iL)/2
RBL
311
321
iL
310
320
322
BL
iL
(iH+iL)/2
RBL
371
372
Comparator
VREF
Comparator
VREF
361
iT
iL
(iH+iL)/2
iT
362
iT-iL
SDL
RSDL
iT-(iH+iL)/2
S/A
380

Fig. 5

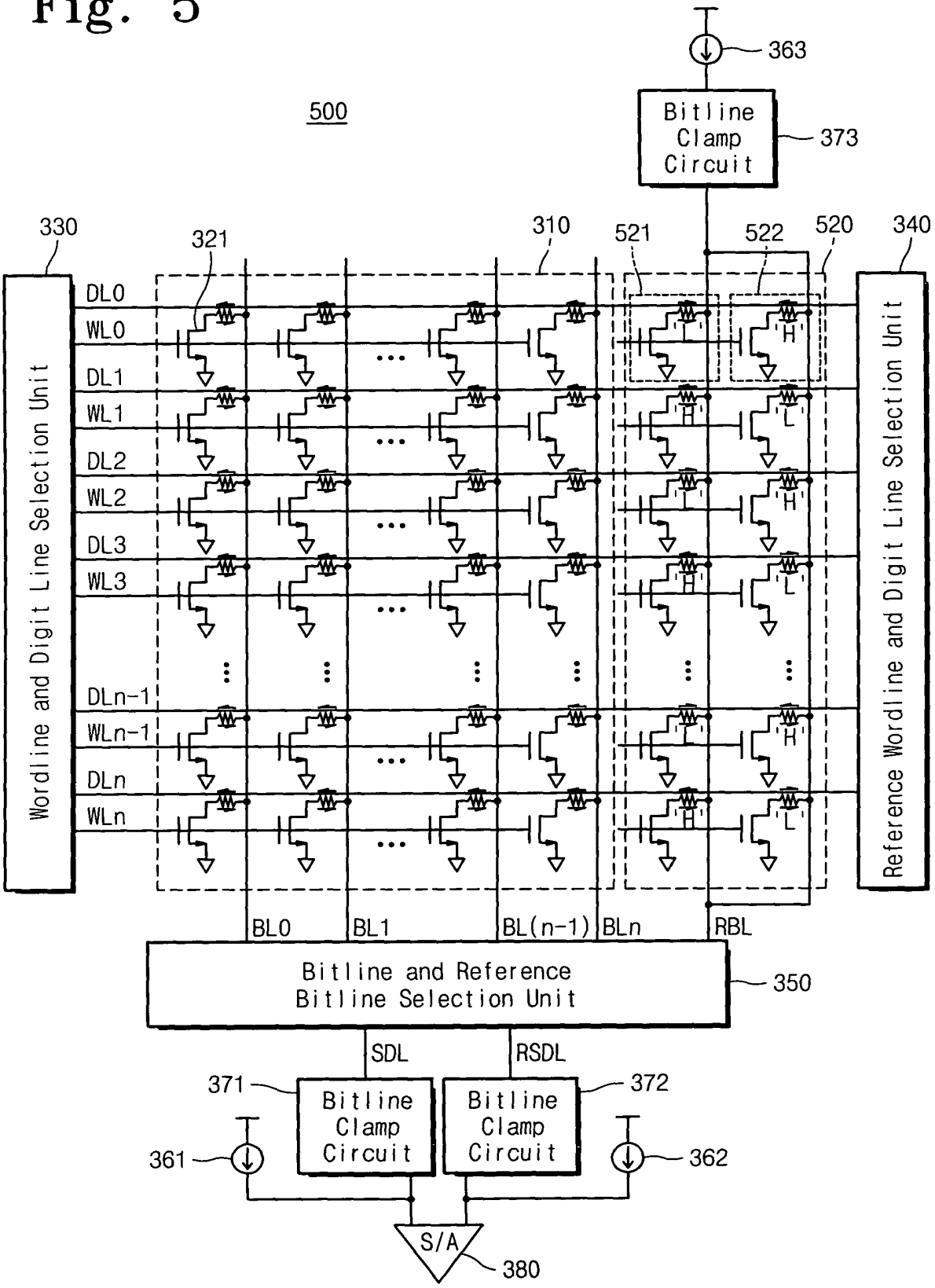
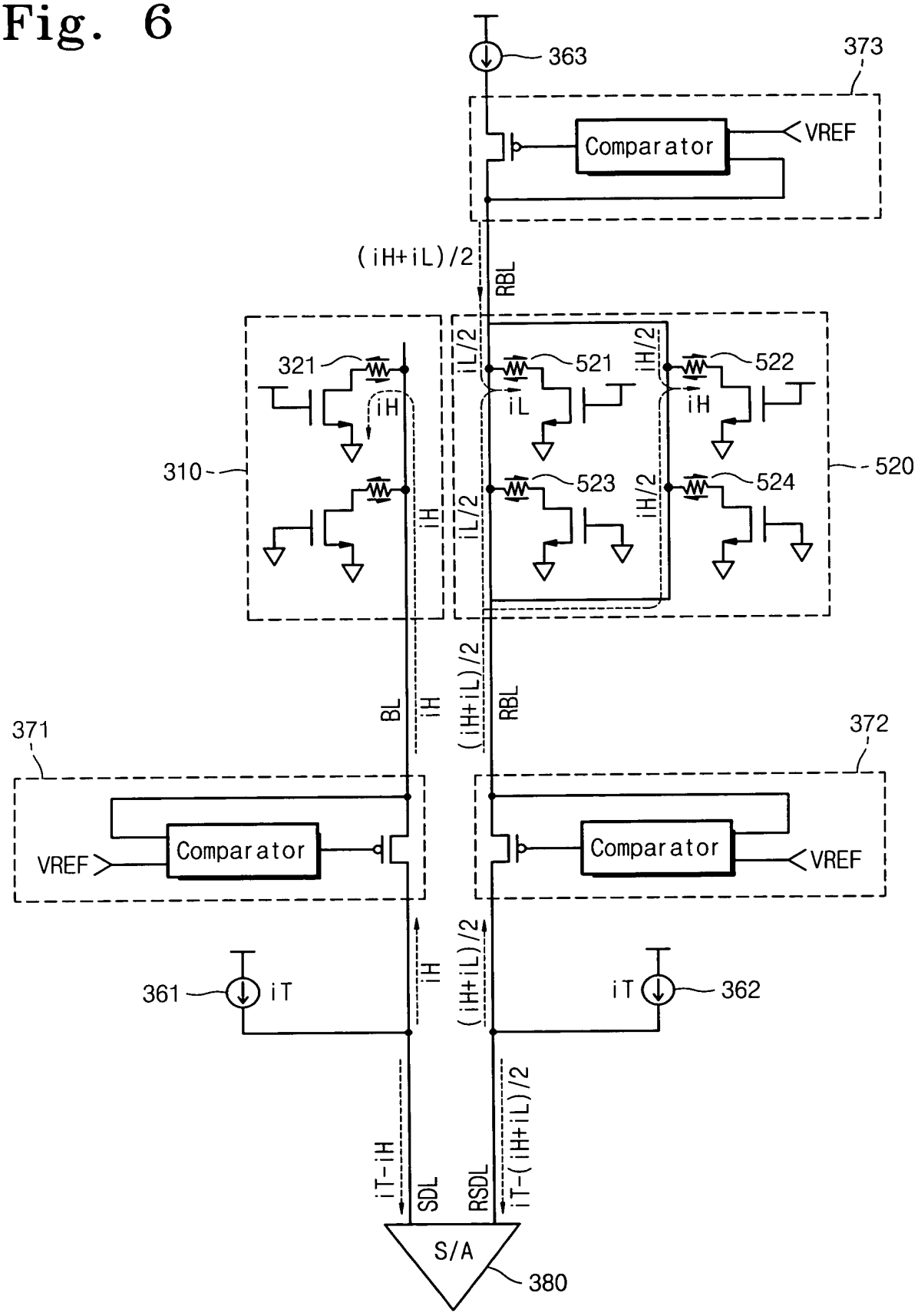

500
363
Bitline Clamp Circuit
373
330
321
310
521
522
520
340
Wordline and Digit Line Selection Unit
Reference Wordline and Digit Line Selection Unit
DL0
WL0
DL1
WL1
DL2
WL2
DL3
WL3
DLn-1
WLn-1
DLn
WLn
H
L
BL0
BL1
BL(n-1)
BLn
RBL
Bitline and Reference Bitline Selection Unit
350
SDL
RSDL
371
372
Bitline Clamp Circuit
Bitline Clamp Circuit
361
362
S/A
380

Fig. 6


363
373
Comparator
VREF
(iH+iL)/2
RBL
321
iH
310
iL/2
521
iL
iH/2
522
iH
520
523
524
iL/2
iH/2
iH
BL
iH
(iH+iL)/2
RBL
371
372
Comparator
VREF
Comparator
VREF
361
iT
iH
(iH+iL)/2
iT
362
iT-iH
SDL
RSDL
iT-(iH+iL)/2
S/A
380